REMARKS

The claims are claims 1, 3, 4, 6 to 9 and 11.

The application has been amended at several locations to correct minor errors in correspondence between reference numeral used in the text and the drawings.

Claims 1 and 6 are amended. Claims 2, 5 and 10 are canceled. Claim 1 is amended to include subject matter previously recited in canceled claim 5. Claim 6 is similarly amended to include subject matter previously recited in canceled claim 10. This subject matter is clarified to distinguish over the references.

Claim 5 (corresponding to amended claim 1) was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Sayegh U.S. Patent No. 5,293,330, Brockmeyer et al U.S. Patent No. 6,591,284 and Shridhar et al U.S. Patent No. 6,366,937.

Amended claim 1 recites subject matter not made obvious by the combination of Sayegh, Brockmeyer et al and Shridhar et al. Claim 1 recites "disposing said input data into memory, each R continuous data set in continuous memory locations with a space in memory locations from an end of one continuous data set to a beginning of a next continuous data set equal to the size of a cache line." The OFFICE ACTION cites column 9, lines 58 to 60 of Shridhar et al as making obvious a similar limitation recited in original claim 5. Shridhar et al states at column 9, lines 53 to 69 (including the portion cited in the OFFICE ACTION):

> "In a preferred embodiment, the processor ahs a prefetch instruction which is used to load the eight values of the twiddle factors into the cache memory. Each time the twiddle factors are loaded into the matrix registers, the prefetch instruction is executed in the background to prefetch the next eight twiddle factors. Each cache-line of the cache stores thirty-two bytes which is sufficient to store all eight values of the twiddle factors."

The Applicant respectfully submits that this disclosure of Shridhar et al includes no teaching on how the twiddle factors are stored in memory. This portion of Shridhar et al teaches a prefetch instruction to fetch a next set of twiddle factors and that eight twiddle factors can be stored in a cache line. Such a prefetch instruction triggered by loading values implies the twiddle factors are in continuous memory locations. This fails to make obvious the space in memory locations recited in amended claim 1. This application teaches at page 29, line 13 to page 33, line 5 that this alignment of data in memory avoids many cache conflict misses by assuring that the four input elements of a butterfly map to different cache sets. This application teaches that this mapping to different sets is a consequence of this memory alignment and prevents conflict misses. Accordingly, claim 1 is allowable over the combination of Sayegh, Brockmeyer et al and Shridhar et al.

Claim 10 (corresponding to amended claim 6) was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Wadleigh U.S. Patent No. 6,088,714, Sayegh U.S. Patent No. 5,293,330 and Shridhar et al U.S. Patent No. 6,366,937.

Claim 6 recites subject matter not made obvious by the combination of Wadleigh, Sayegh and Shridhar et al. Claim 6 recites "disposing said input data into memory, each R continuous data set in continuous memory locations with a space in memory locations from an end of one continuous data set to a beginning of a next continuous data set equal to the size of a cache line." The OFFICE ACTION cites column 9, lines 58 to 60 of Shridhar et al as making obvious a similar limitation recited in original claim 10. The Applicant respectfully submits that this disclosure of Shridhar et al (quoted above) includes no teaching on how the twiddle factors are stored in memory. This portion of Shridhar et al teaches a prefetch instruction to fetch a next set of twiddle factors and that eight twiddle factors can be stored in a cache

line. Such a prefetch instruction triggered by loading values implies the twiddle factors are in continuous memory locations. This fails to make obvious the space in memory locations recited in amended claim 1. This application teaches at page 29, line 13 to page 33, line 5 that this alignment of data in memory avoids many cache conflict misses by assuring that the four input elements of a butterfly map to different cache sets. This application teaches that this mapping to different sets is a consequence of this memory alignment and prevents conflict misses. Accordingly, claim 6 is allowable over the combination of Wadleigh, Sayegh and Shridhar et al.

Claim 6 recites further subject matter not made obvious by the combination of Wadleigh, Sayegh and Shridhar et al. Claim 6 recites steps of performing a first stage radix-R butterfly computation and successively performing second and subsequent state butterfly computations "if said data set is larger than said data cache but smaller than R times the data cache." The OFFICE ACTION cites column 2, lines 65 to 67 of Wadleigh as making obvious this subject matter. Wadleigh states at column 2, lines 65 to 67:

> "Therefore, there is a need in the art for a FFT mechanism that reduces the number of cache misses that occur when the data block is larger than ⅓ of the size of the cache."

The above quoted limitation in claim 6 includes two bounds on the relationship between the size of the data set and the size of the data cache. The first is a lower bound; the data set must be "larger than said data cache." The second is an upper bound; the data set must be "smaller than R times the data cache." The cited portion of Wadleigh includes only a lower bound, the data block "is larger than ⅓ of the size of the cache." Thus the cited portion of Wadleigh includes a different lower bound on the data set size than

recited in claim 6 and fails to include any upper bound on this data set size. Thus this limitation taught in Wadleigh fails to make obvious either the lower bound or the upper bound recited in claim 6. The OFFICE ACTION includes no argument how the limitation taught in Wadleigh makes obvious this different limitation in claim 6. Accordingly, claim 6 is allowable over the combination of Wadleigh, Sayegh and Shridhar et al.

Claim 11 was rejected under 35 U.S.C. 103(a) as made obvious by the combination of Wadleigh U.S. Patent No. 6,088,714 and Sayegh U.S. Patent No. 5,293,330. Paragraph 11 of the OFFICE ACTION applies the same reasoning in the rejection of claim 6 to claim 11.

Claim 11 recites subject matter not made obvious by the combination of Wadleigh and Sayegh. Claim 11 recites two limitations "if said data set is larger than R times the data cache" that differ from the two limitations recited in claim 6 "if said data set is larger than said data cache but smaller than R times the data cache." The OFFICE ACTION cites column 2, lines 65 to 67 of Wadleigh as teaching steps in original claim 6 preformed "if said data set is larger than said data cache but smaller than R times the data cache." This portion of Wadleigh is quoted above. The Applicant respectfully submits that this portion of Wadleigh teaches a different lower bound on the data set size "larger than ⅓ of the size of the cache" than recited in claim 11 "larger than R times the data cache." The OFFICE ACTION includes no argument how the limitation taught in Wadleigh makes obvious this different limitation in claim 11. Accordingly, claim 6 is allowable over the combination of Wadleigh and Sayegh.

Claims 3 and 4 are allowable by dependence upon allowable claim 1.

Claims 7 to 9 are allowable by dependence upon allowable claim 6.

The Applicants respectfully submit that all the present claims

are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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